

TOSHIBA MOS INTEGRATED CIRCUIT SILICON GATE CMOS

8 MBIT (512 K WORD BY 16 BITS/1 M WORD BY 8 BITS) CMOS MASK ROM

DESCRIPTION

The TC538200AP/AF is a 8,388,608-bit Read Only Memory organized as 524,288 words by 16 bits when BYTE is logical high, and as 1,048,576 words by 8 bits when BYTE is logical low.

The TC538200AP/AF is most suitable for application such as program memory, data memory fast high speed from, and character generators.

The TC538200AP/AF is packaged in a standard 600 mil 42-pin DIP or 600 mil 44-pin SOP or 400 mil 44-pin TSOP Type II.

FEATURES

- Single 5 V Power Supply
- Access Time: 150 ns (max)
- Power Dissipation
 - Operating Current: 60 mA (max)
 - Standby Current : 100 μ A (max)
- Fully Static Operation
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- TC538200AP: DIP42-P-600
- TC538200AF: SOP44-P-600
- TC538200AFT: TSOP44-P-400

PIN ASSIGNMENT (TOP VIEW)

A18	1	42	NC	A18	2	43	NC
A17	2	41	A8	A17	3	42	A8
A7	3	40	A9	A7	4	41	A9
A6	4	39	A10	A6	5	40	A10
A5	5	38	A11	A5	6	39	A11
A4	6	37	A12	A4	7	38	A12
A3	7	36	A13	A3	8	37	A13
A2	8	35	A14	A2	9	36	A14
A1	9	34	A15	A1	10	35	A15
A0	10	33	A16	A0	11	34	A16
CE	11	32	BYTE	CE	12	33	BYTE
GND	12	31	GND	GND	13	32	GND
OE	13	30	D15/A - 1	OE	14	31	D15/A - 1
D0	14	29	D7	D0	15	30	D7
D8	15	28	D14	D8	16	29	D14
D1	16	27	D6	D1	17	28	D6
D9	17	26	D13	D9	18	27	D13
D2	18	25	D5	D2	19	26	D5
D10	19	24	D12	D10	20	25	D12
D3	20	23	D4	D3	21	24	D4
D11	21	22	V _{DD}	D11	22	23	V _{DD}

TC538200AP

TC538200AF

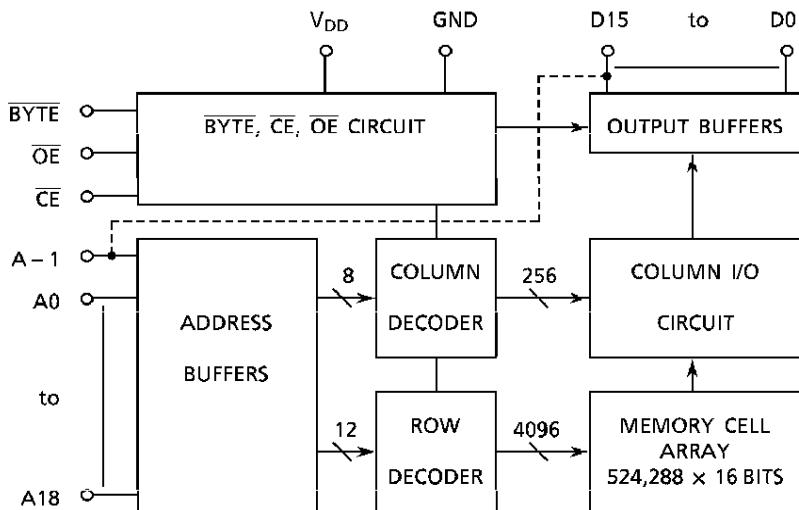
TC538200AFT

PIN NAMES

A0 to A18	Address Inputs
D0 to D14	Data Outputs
CE	Chip Enable Input
OE	Output Enable Input
D15/A - 1	Data Output/Address Input
BYTE	Word, Byte Selection Input
V _{DD}	Power Supply
GND	Ground
NC	No Connection

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BLOCK DIAGRAMMODE SELECTION

MODE	CE	OE	BYTE	D0 TO D7	D8 TO D14	D15/A-1	POWER
Read (16-Bit)	L	L	H	Data Out			Active
Read (8-Bit)	L	L	L	Data Out (Lower 8 bits)	High Impedance	L	Active
Read (8-Bit)	L	L	L	Data Out (Upper 8 bits)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H: VIH L: Vil *: VIH or Vil

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.5 to 7.0	V
V _{IN}	Input Voltage	- 0.5 to V _{DD}	V
V _{OUT}	Output Voltage	0 to V _{DD}	V
P _D	Power Dissipation	1.0/0.6*	W
T _{STG}	Storage Temperature	- 55 to 150	°C
T _{OPR}	Operating Temperature	0 to 70	°C
T _{SOLDER}	Soldering Temperature (10 s)	260	°C

* SOP/TSOP

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ$ to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3	-	0.8	V

DC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0$ to V_{DD}	-	± 1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ to V_{DD}	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{ V}$	- 1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{ V}$	2.0	-	mA
I_{DDS1}	Standby Current	$\bar{CE} = V_{IH}$	-	2	mA
I_{DDS2}		$\bar{CE} = V_{DD} - 0.2\text{ V}$	-	100	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 150\text{ ns}$	-	70	mA
I_{DDO2}		$V_{IN} = V_{DD} - 0.2\text{ V}/0.2\text{ V}, t_{cycle} = 150\text{ ns}$	-	60	mA

CAPACITANCE ($f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{ V}$	-	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{ V}$	-	12	pF

Note: This parameter is periodically sampled and is not tested for every component.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

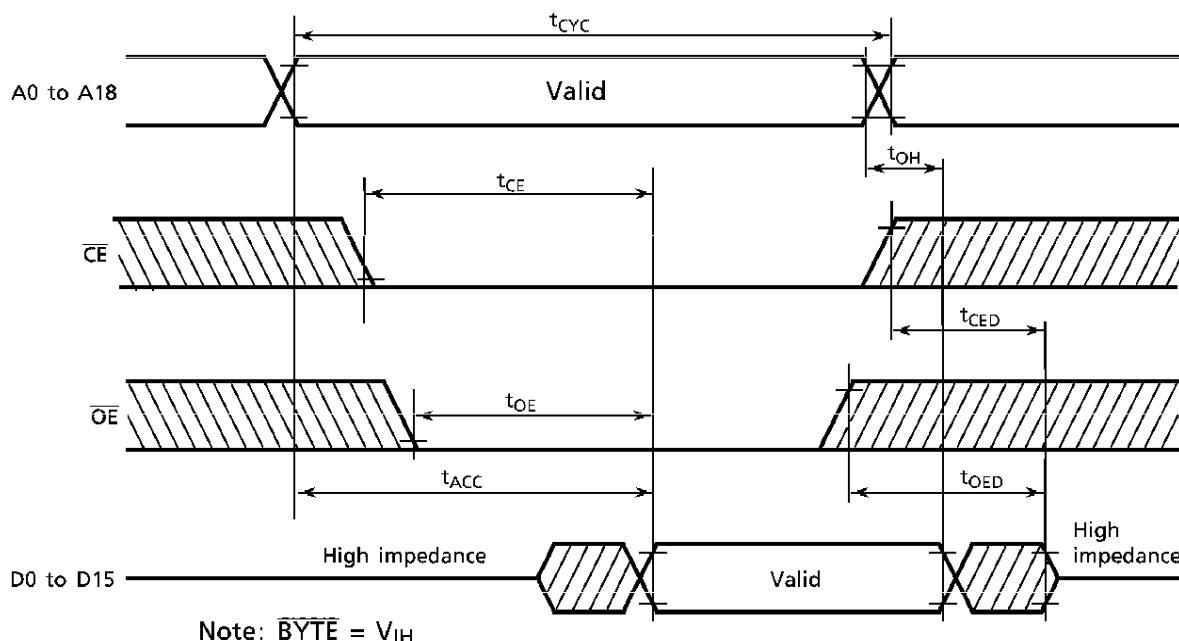
SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{CYC}	Cycle Time	150	—	ns
t _{ACC}	Address Access Time	—	150	ns
t _{CE}	Chip Enable Access Time	—	150	ns
t _{BT}	BYTE Access Time	—	150	ns
t _{OE}	Output Enable Access Time	—	70	ns
t _{CED}	Output Disable Time from \overline{CE}	—	60	ns
t _{TOED}	Output Disable Time from \overline{OE}	—	60	ns
t _{BTD}	Output Disable Time from BYTE	—	60	ns
t _{OH}	Output Hold Time	5	—	ns

AC TEST CONDITIONS

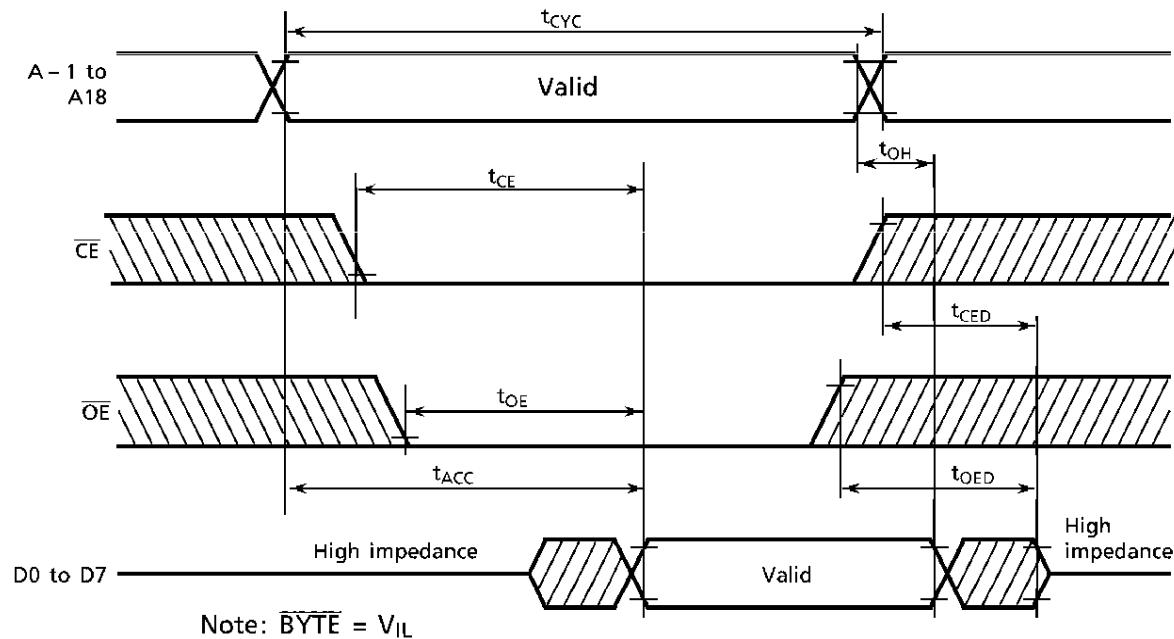
Output Load : 100 pF + 1 TTL
 Input Levels : 0.6 V, 2.4 V
 Timing Measurement Reference Levels
 Input : 0.8 V, 2.2 V
 Output: 0.8 V, 2.0 V
 Input Rise and Fall Time : 5 ns

TIMING DIAGRAMS

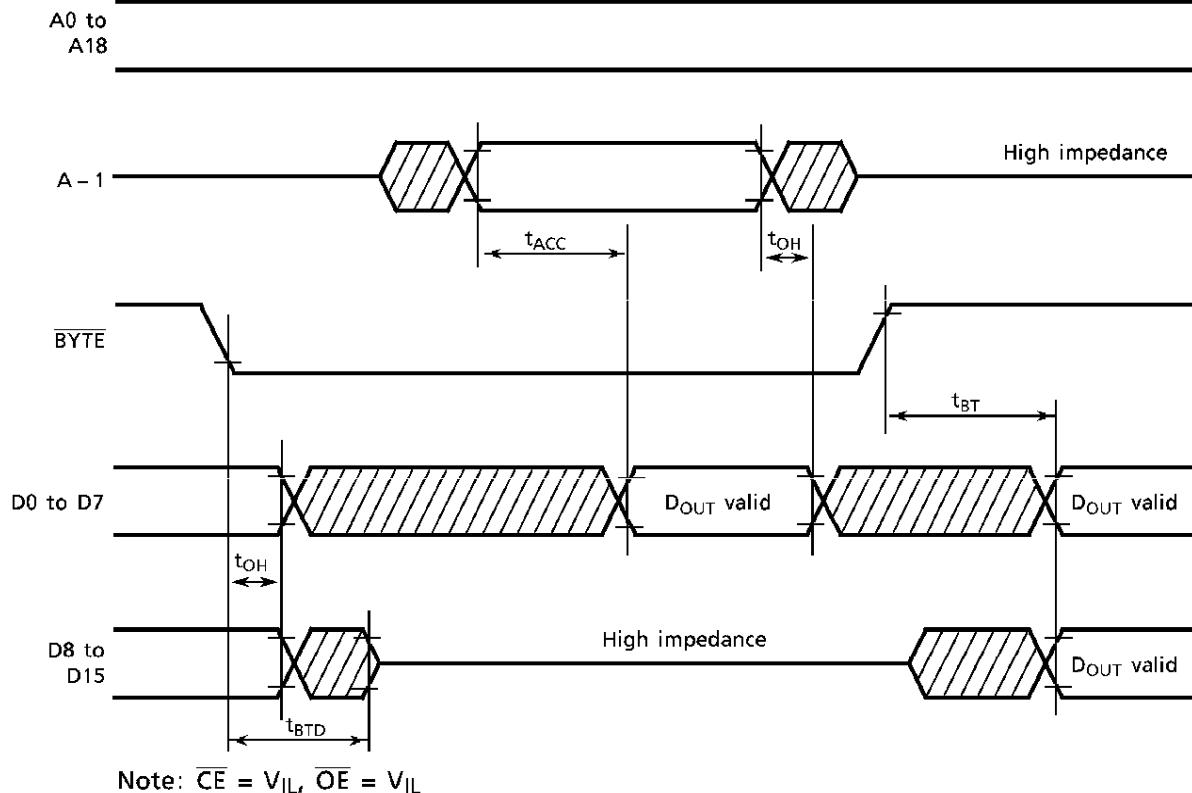
WORD-WIDE READ MODE



BYTE-WIDE READ MODE



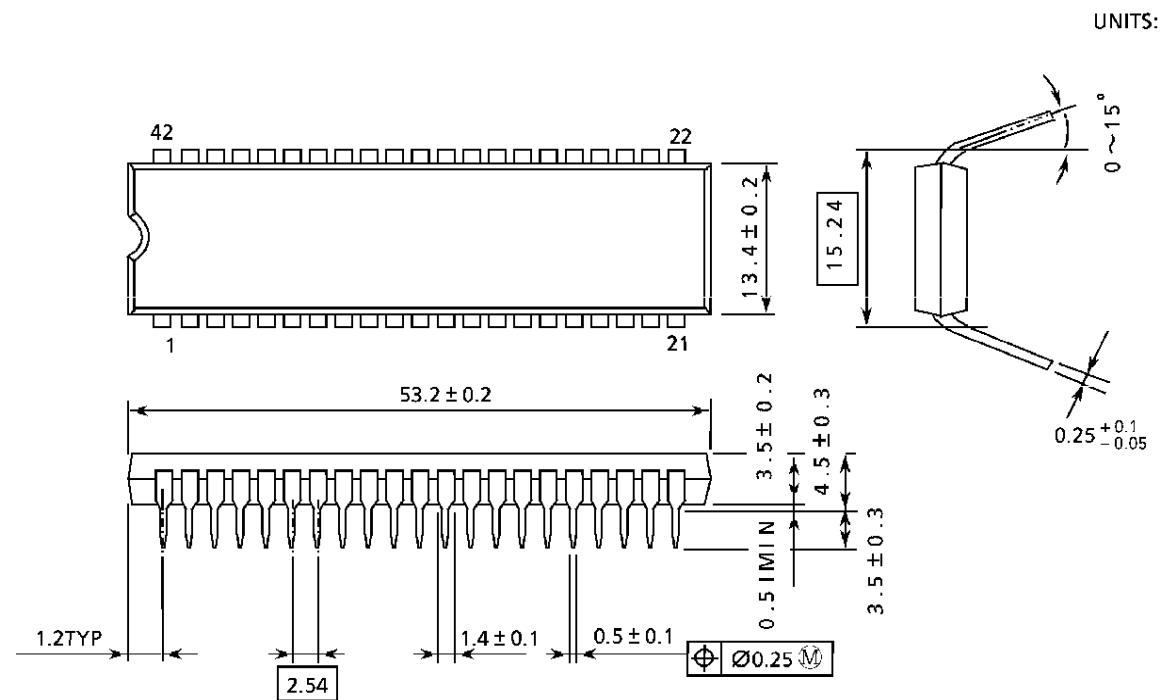
BYTE TRANSITION



PACKAGE DIMENSIONS

● Plastic DIP

DIP42-P-600-2.54



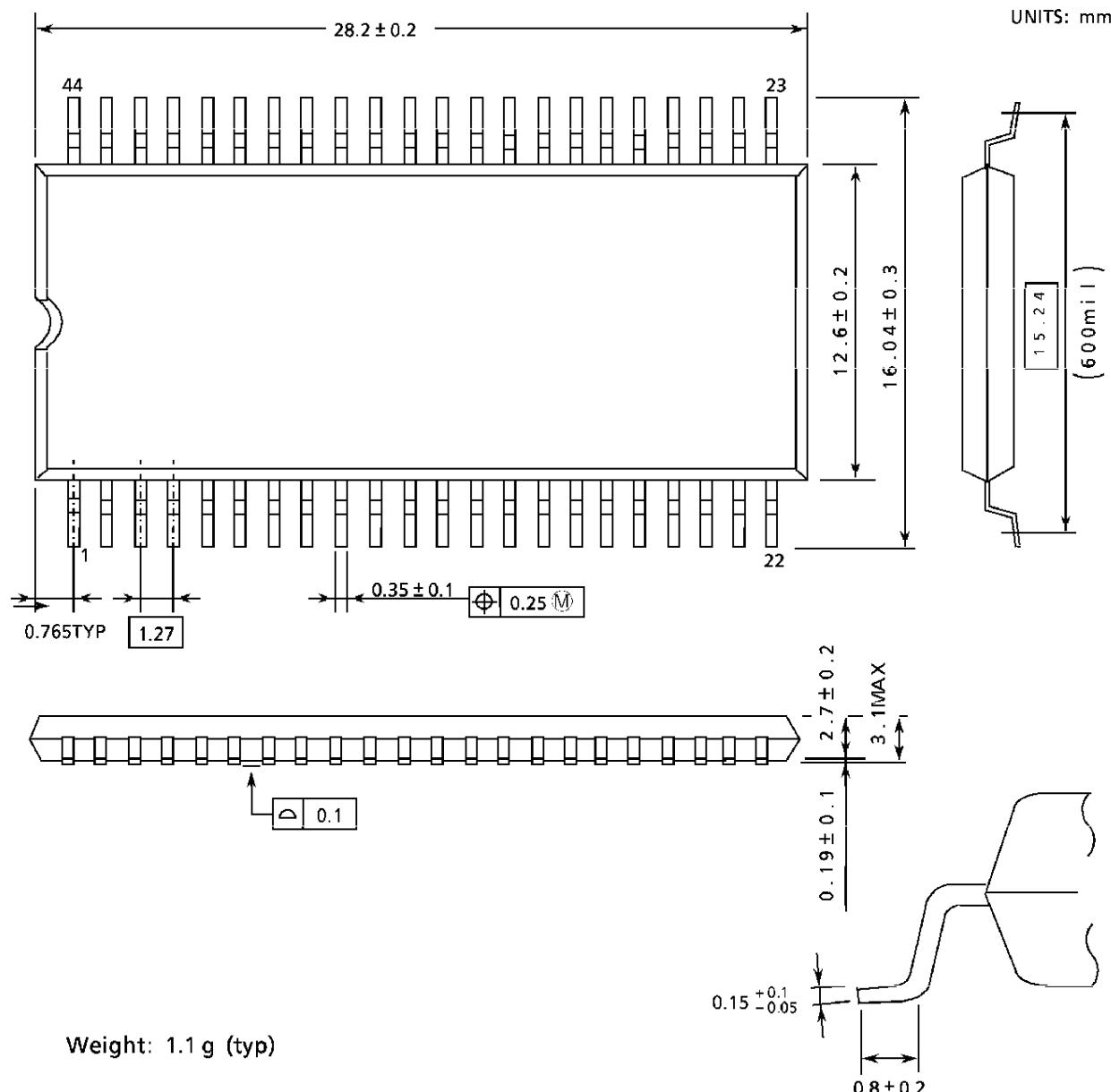
Weight: 5.7 g (typ)

Note: Package width and length do not include mold protrusion. The permissible mold protrusion is 0.15 mm.

PACKAGE DIMENSIONS

- Plastic SOP

SOP44-P-600-1.27

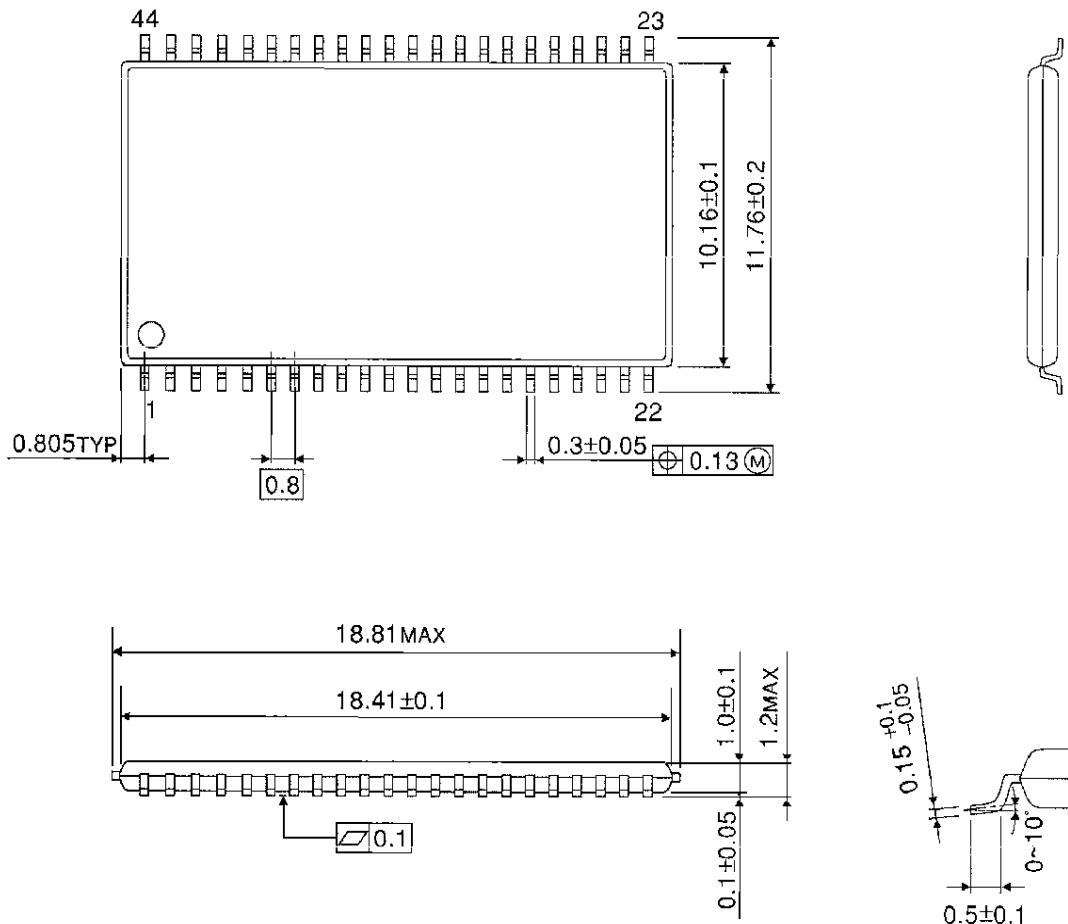


Note: Package width and length do not include mold protrusion. The permissible mold protrusion is 0.15 mm.

PACKAGE DIMENSIONS

- TC534200CFT

TSOP II 44-P-400-0.80



Weight : 0.5g (Typ)